What is claimed is:

Sub A3

1. A data processing device comprising:

a plurality of connection terminals for being individually supplied with signals including processing data, a clock signal, and a reset signal, and drive electric power;

at least one radio antenna for receiving said signals and said drive electric power as one radio wave;

a data processing circuit switchable between a terminal mode in which only the signals supplied to said connection terminals are effective and an RF mode in which only the radio wave supplied to said radio antenna is effective, said data processing circuit being supplied with said drive electric power and said signals; and

a mode selecting circuit for setting said data processing circuit to said RF mode by default in response to said drive electric power starting to be supplied, and for switching to said terminal mode in response to the clock signal and the reset signal which are applied to corresponding ones of said connection terminals.

2. A data processing device according to claim 1, wherein said mode selecting circuit has mode maintaining means for maintaining said terminal mode until the supply of said drive electric power is stopped.

3. A data processing device according to claim 1, wherein said mode selecting circuit comprises:

clock counting means for counting clock pulses of the clock signal supplied in response to said drive electric power starting to be supplied; and

input deciding means for outputting a switching signal to switch said data processing circuit to said terminal mode when said clock counting means has counted a predetermined number of clock pulses.

4. A data processing device according to claim 3, wherein said input deciding means has data output means for outputting said reset signal as said switching signal when said clock counting means has counted a predetermined number of clock pulses.

5. A data processing device according to claim 3, wherein said mode selecting circuit has mode maintaining means for applying said switching signal output by said input deciding means as a dummy clock

signal to said clock counting means through a feedback loop.

Add A2

Add B7